
13. Circuit Operating Descriptions

13-1 Power Supply (Free Voltage)

13-1-1 Circuit explanations

1) Power AC input Rectification/Smoothing Terminal

- ❶ The conversion of AC power to DC (An electric wave rectification)
- ❷ PC10 : Voltage has smoothing by DC converted.
- ❸ PC2, PC11, PL2 : The use of removing input/ output noise of power terminal.
- ❹ PR10 : When power code is inserted, the restriction resistor of Inrush current.
 - When there is no PR1, Inrush current is ON that the cause of bridge diode broken.

2) Snubber circuit : PD5, ZD2

- ❶ When the switch is off, It prevents switch both terminal to occurrence a higher voltage / Suppressing the occurrence of noise.
 - Trans 1st winding is coil, when cut off current the occurrence of higher counter electromotive force.
- ($V = -LI * (di/dt)$) (LI : LEAKAGE INDUCTANCE)
- Dt is very short time, in actuality circuit similarly with fig 13-1, occurrence very high voltage on PL2 both terminal. Snubber circuit is damage protection of IC01 through Leakage voltage control by Zener Diode.

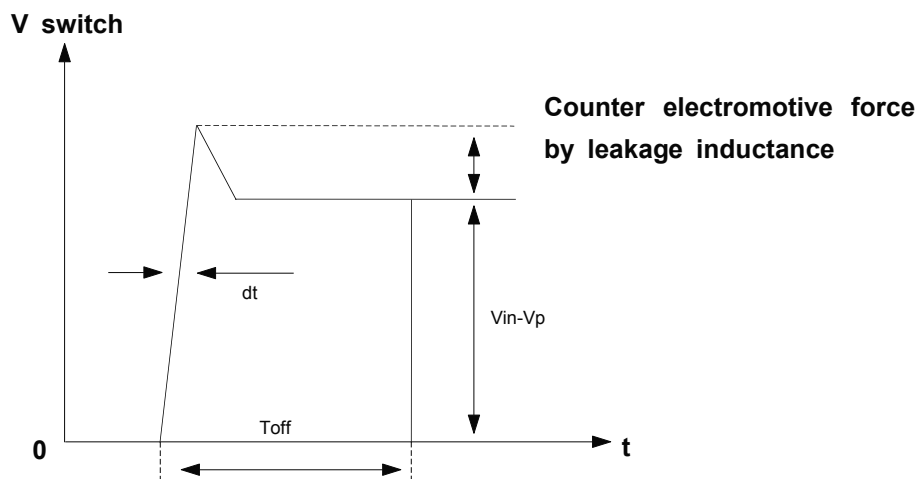


Fig 13-1

3) Switching IC (IC01) Vcc the circuit

- ❶ PR11, PR12, PR13 : Q2's motive resistor.
[When power code inserted that Q2 operating per motive resistor]
- ❷ IC1 Vcc : PD10, PR16
 - After IC1 is motivated that current begins to pass to trans. So use trans output by Vcc
 - The trans output is AC, rectification by PD9, smoothing by PC11
 - The reasons that use trans output by IC1 Vcc : The load is difference with before and after of IC1.
[Load will be raised after operation, Only if motive resistor is used, the Vcc of IC1 will be Down under the OFF Voltage so, it's impossible to work]
- ❸ PC13, PC14 : Remove noise

4) SWITCHING IC (IC1) Description : PWM IC

Table 13-1

Pin No.	Pin Name	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	Isense	Controller Current Sense Input,
		CoolMOS Source Output
4	Drain	650V CoolMOS Drain
5	Drain	650V CoolMOS Drain
6	N.C	Not connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

5) Feedback Control Circuit

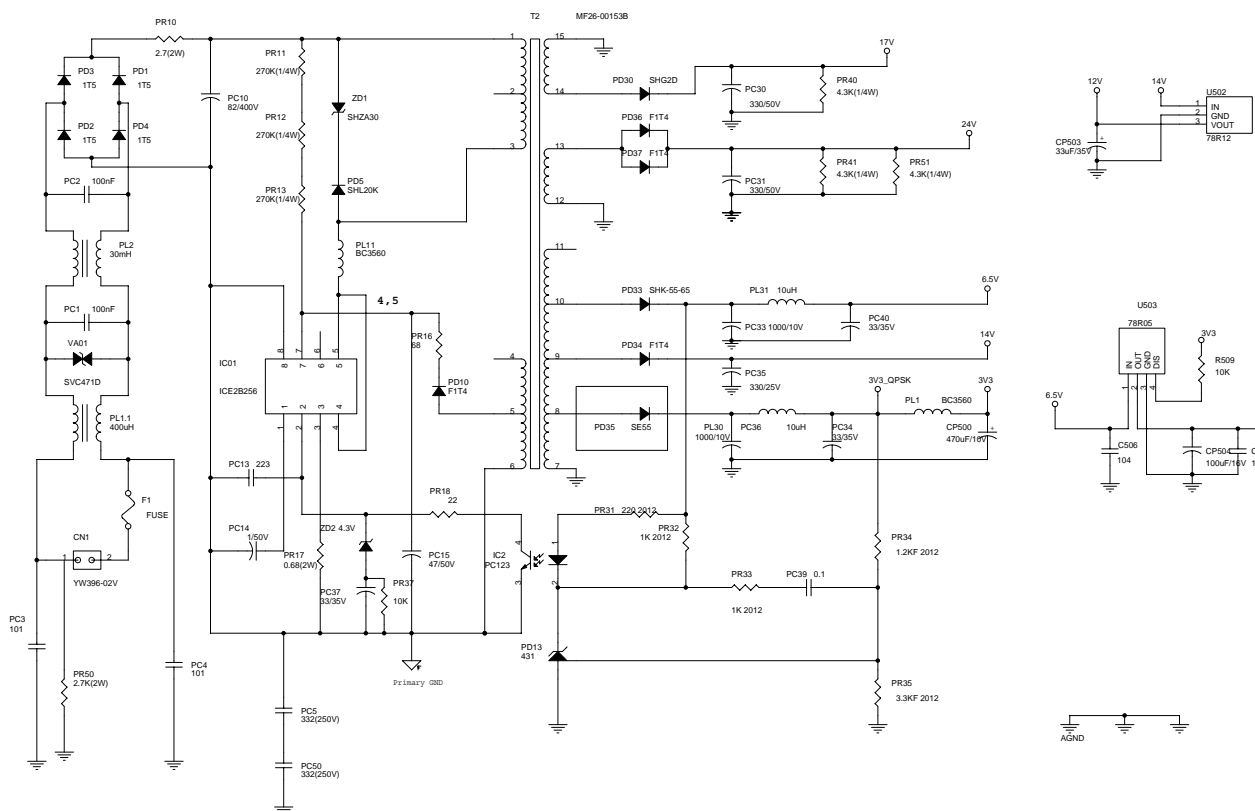


Fig 13-2

5-1) operation of description

- ❶ F/B terminl of IC1 has decided output a cycle.
- ❷ When the F/S terminal node is open : Intermittents operation.
(OCP : Over current protect motion) mode.
 - F/B potential is fixed by 7.5V interiorly.When normal operated, the F/B potential is adjusted by 0.4~7.5V per C-E voltage of IC2.
 - When the F/B terminal is open that it's intermittents operating for 7.5V.

5-2) When DC output of load is alter that circuit operation descriptions.

- ❶ Internal OP Amp of PD13. + standard potential is 2.5V, It's connected to keep up the DC STB +3.3V by PR34 with PR35.
- ❷ In case down of under STB +3.3V, +6V, +30V which DC output load is increased (or decrease with AC input voltage); PD13 of Verf potential become down by under 2.5V, PD13 of A-K's current decrease.
A-K of IC1 current decrease --> IC2 Diode current decrease --> C-E of IC2 current decrease --> IC2 of C-E voltage crease --> Increase in IC01 F/S voltage --> Increase in Out Duty --> 1st current of trans is increase --> 1st Power of trans is increase --> Increase in DC output --> DC output STB +3.3V, +6V, +24V maintain.
- ❸ In case over increase that DC output load to be decrease (or AC input voltage increase) STB +3.3V, +6V, +24V
-->As above description with contrariwise analysis --> Diminution of Duty
-->DC output STB+3.3V, +6V, +24V maintain.
- Exactly, always doing feedback control to maintain STB+3.3V, +6V, +24V
- ❹ Each elements operating function
- PR31, PR32 : DC output overshoot decrease a part
- PC39 : IC01 Oscillator prevention (Phase a correction)

6) OCP limitation circuit

- ❶ Contruction of the circuit : IC01 interior circuit by itself.
- ❷ A part : SWITCH (IC01) over current, over load protection.

6-1) Intermittence operation : It'll happens that IC1 cann't do regular output and appearance in repeating.

Typical an example) DC Output short and Feedback circuit open

- DC Output Short --> 2nd load is concentration by Short terminal --> DC output voltage down
-->F/B voltage rising -->Increase in Duty -->Increase in switch current-->Internal IC switch current restriction (Duty restriction)-->The 1st supply load is less than the 2nd load -->IC1 Vcc terminal of output voltage was under 8.4V down -->IC1 ON per motive resistor -->Repetitive operation as above -->maintain intermittence operation mode)

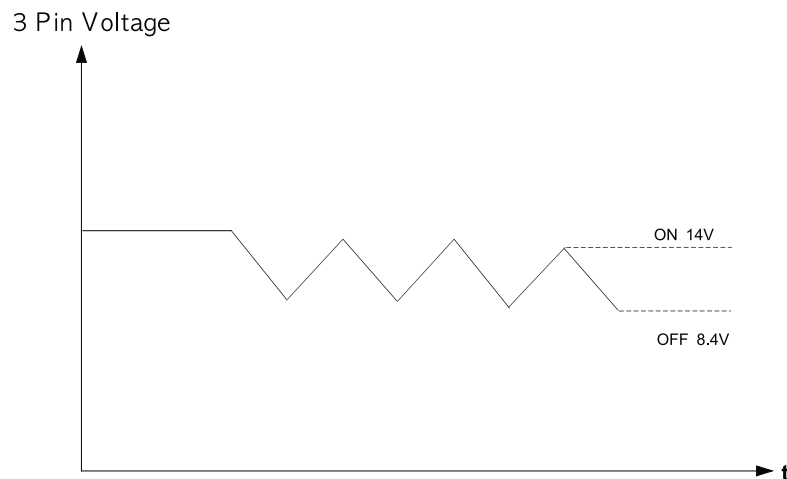


Fig 13-3

13-2 Main Processor Description

13-2-1 Overview

The central processing unit(CPU) is the ST202+32bit processor core.It contains instruction processing logic, instruction and data pointers, and a three registers evaluation stack.It can directly access the high speed on-chip memory,which can store data or programs.Where larger amounts of memory are required,the processor provides high performance:

◆ The ST20-C201 processor core is 166MHz, 2 Kbyte instruction cache, 2 Kbyte data cache and 4 Kbyte SRAM.

13-2-2 Transport stream processing

1) Overview

The STi5518 contains a programmable transport interface block(PTI) for concurrent demultiplexing and descrambling of transport streams.Transport streams are input via the parallel/serial TS inputs.A second parallel TS input interface is available via the link layer interface if neither IEEE1284 nor a transport stream output is required.

2) Transport stream input/output

A single transport stream is routed to the PTI by the TSMUX block.Any of the three externally supplied input streams can be routed to the PTI.This is illustrated in Fig 13-4.

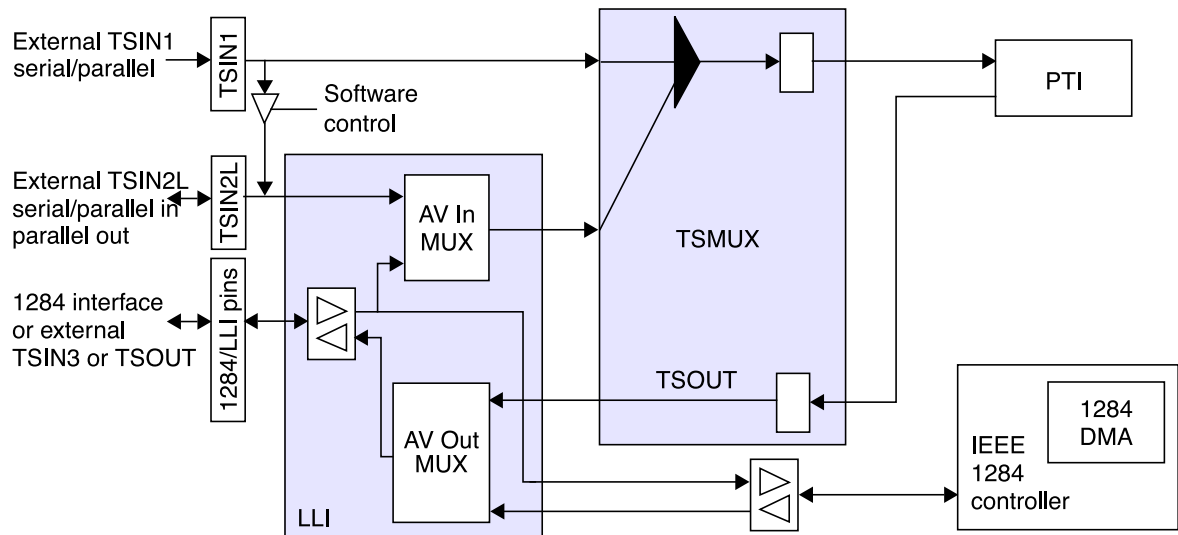


Fig 13-4 TSMUX input and outputs

13-2-3 MPEG graphics and display architecture

The MPEG graphics and display architecture shown in the following diagram provides the graphics, videostream processing and display capabilities of the STi5518.

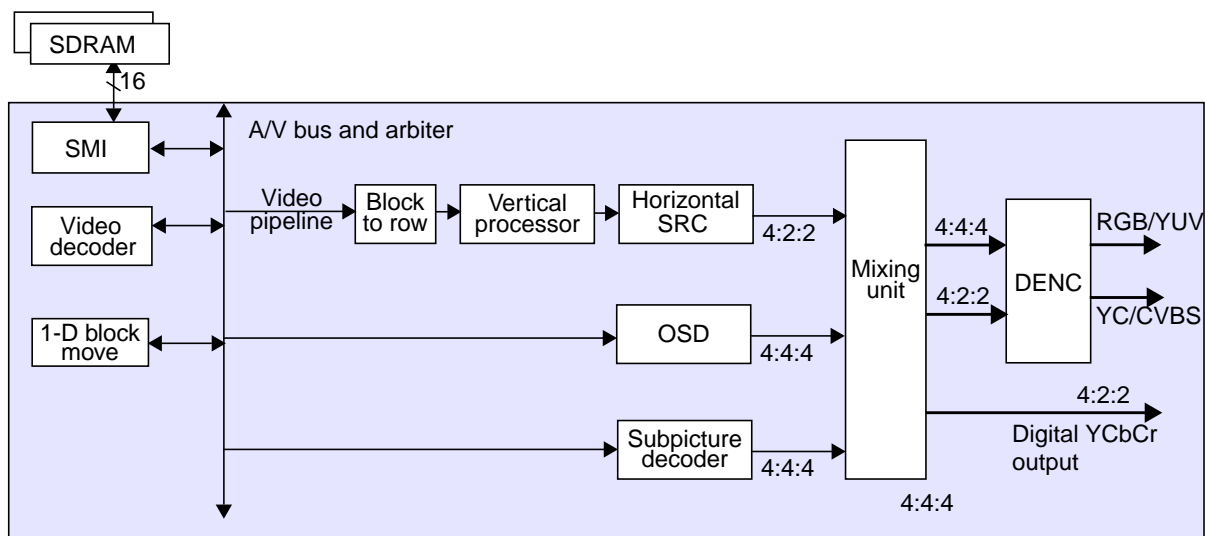


Fig 13-5 Graphics and display subsystem

13-2-4 Memory map

1) Overview

The STi5517 memory space is divided into four main regions:

- ◆ region 0 : Addresses which map on to the on-chip SRAM.
- ◆ region 1 : Addresses which map on to the off-chip SDRAM connected to the local SMI.
- ◆ region 2 : Addresses which map on to the on-chip peripheral configuration registers.
- ◆ region 3 : Addresses which map on to the external memory interface(EMI).

Region 3 is decoded via the EMI buffer into six banks,the boundaries between these banks can be programmed using six configuration registers.Addresses bits 29 down to 22 are compared with the programmed values to determine the bank of the current access.

The largest programmable size of a bank is 256 Mbytes.The minimum is 4 Mbytes.

Fig 13-6 illustrates the top level address map breakdown.

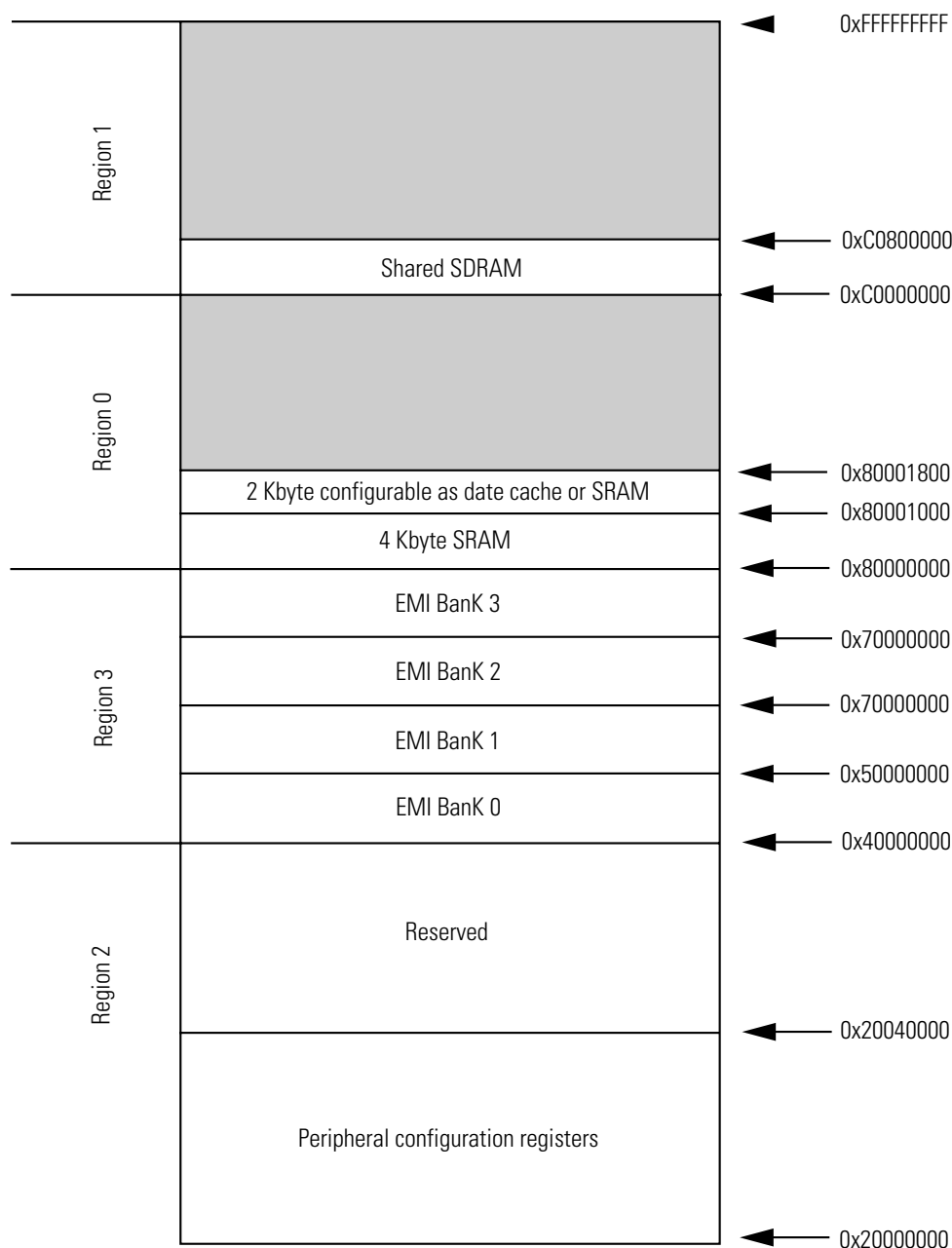


Fig 13-6 Illustrates the top level address map breakdown

13-2-5 MPEG video decoder

1) Overview

The MPEG video decoder decompresses an MPEG 2-bit stream and constructs a picture.

The video decoder is a picture decoder; it decodes one picture and then stops until instructed to decode the next picture in the video bit stream.

Normally, the decoding of a new picture starts in response to the start of display of a new picture. The registers whose contents can change from picture to picture are double banked and are updated automatically when decoding starts.

2) PES parser

The PES parser is situated between the ST20 arbiter/bus and the compressed data FIFO of the video/audio core. It has a 100 Mbps (maximum burst) bit rate, and allows the following input streams:

- ◆ MPEG-2 PES (Packetized PES), ISO 13818-1.
- ◆ MPEG-1 system layer (ISO 11172-1).

The MPEG-2 PES and MPEG-1 system parser accepts PES streams in the same way that pure audio or video streams are accepted.

For packetized elementary stream data which is demultiplexed from a transport stream (MPEG-2), the data stream consists of concatenated, incomplete packets of audio, and video PES. To handle this configuration, the STi5517 contains two separate parsers: one for the audio (audio PES parser in audio decoder) and one for the video (MPEG-2 PES and MPEG-1 system parser).

As the audio or video data is input, it is demultiplexed by each parser and the audio/video streams are placed in their respective buffers. For program stream data or MPEG-1 systems stream data, the audio and video packets are complete so that a single parser (MPEG-2 PES and MPEG-1 system parser) can be used. The packets are internally separated into video and audio streams. If required, the two parsers can still be used but the packets must be separated by the ST20. See Fig 13-7

- ❶ This path can be used for audio MPEG1 system stream decode or audio MPEG2 program stream decode. However, this path is more sensitive to errors retrievals. The MPEG-2 PES and MPEG-1 system parser can not output elementary stream on this path.
- ❷ The audio PES parser is handled by the audio decoder (software parser).

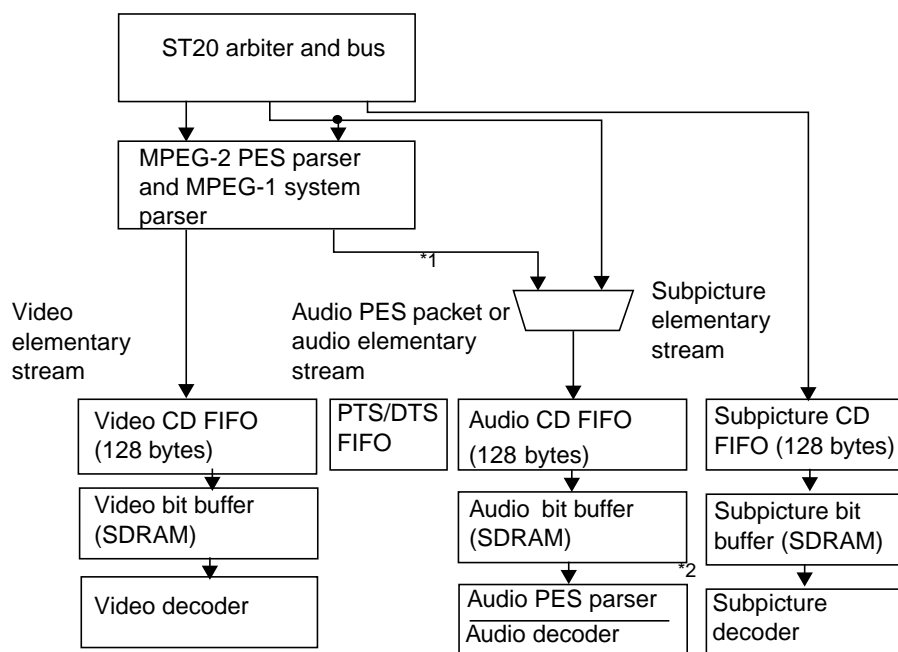


Fig 13-7 System parser internal architecture

3) Display planes

The graphics and display subsystem reads, processes, overlays and mixes pixel data stored in various buffers in SDRAM, and produces a combined image for display on a TV. The buffers are called the display planes.

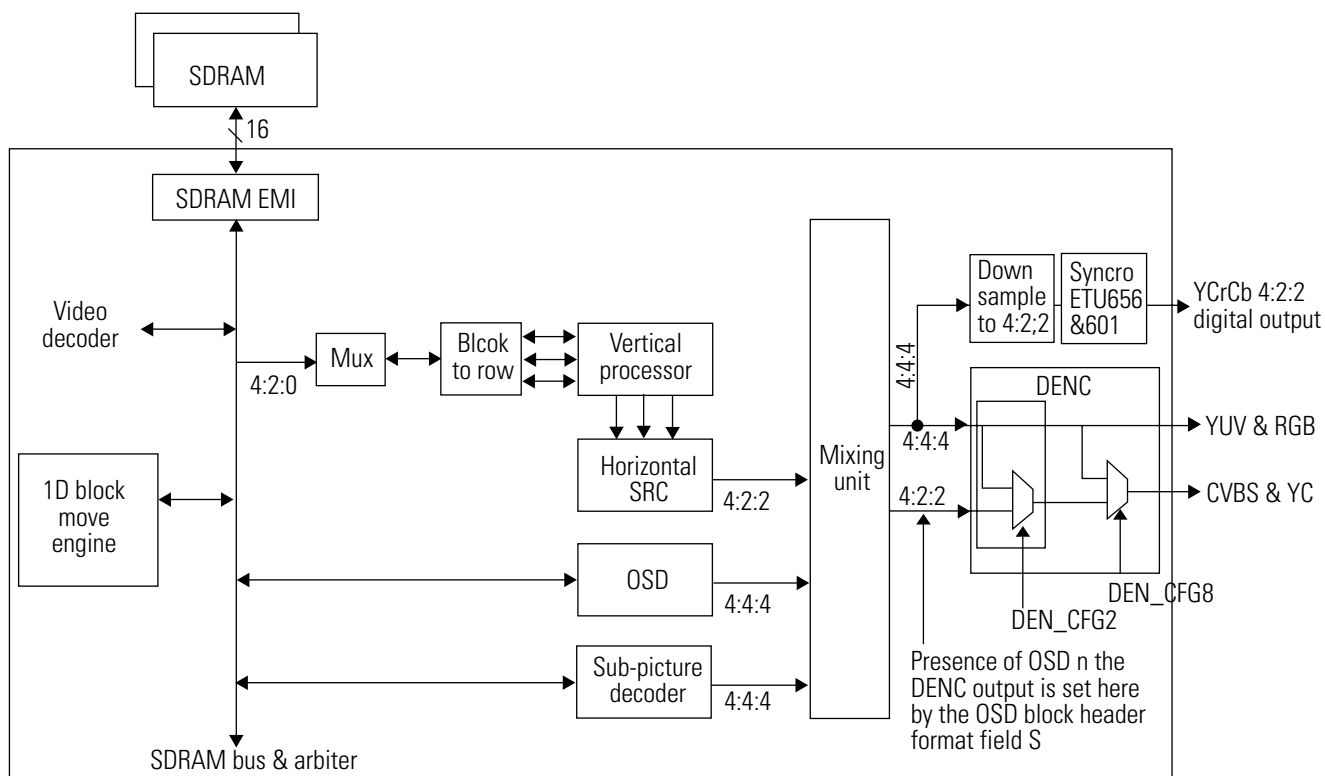


Fig 13-8 Is a simplified block diagram of the graphics and display subsystem.

13-2-6 Audio decoder

1) Overview

The audio decoder accepts:

Dolby® Digital®

- ◆ MPEG-1 layers I and II
- ◆ MP-3(a product variant MPEG-2 Layer 11 6-channel option) (DDA data formats)
- ◆ PCM formats
- ◆ PES streams for MPEG-1 and Dolby® Digital®, MPEG-2, MP3 and linear PCM (LPCM) DIS digital out (DVD DTS and (DDA DTS)

S/PDIF input data(IEC-60958 or IEC-61937 standards) is accepted if external circuitry extracts the PCM clock from the stream and decodes the biphase mark of S/PDIF.

The devices outputs up to four channels of PCM data and appropriate clocks for external digital-to-analog.

- ◆ two PCM data channels on a PCM output(PCMOUT3) for VCR.
- ◆ two PCM data channels on a PCM output(PCMOUT0) for single stereo.
- ◆ three clocks for the external DACs:
 - PCKCLK
 - SCLK
 - LRCLK

Sampling frequencies of FS = 96,48,44.1,32 kHz and half sampling frequencies are supported.

A downsampling filter (96/48 kHz) for PCM data is available. MP3 also supports sampling frequencies of 24,22.05,16,11.025 and 8 kHz.

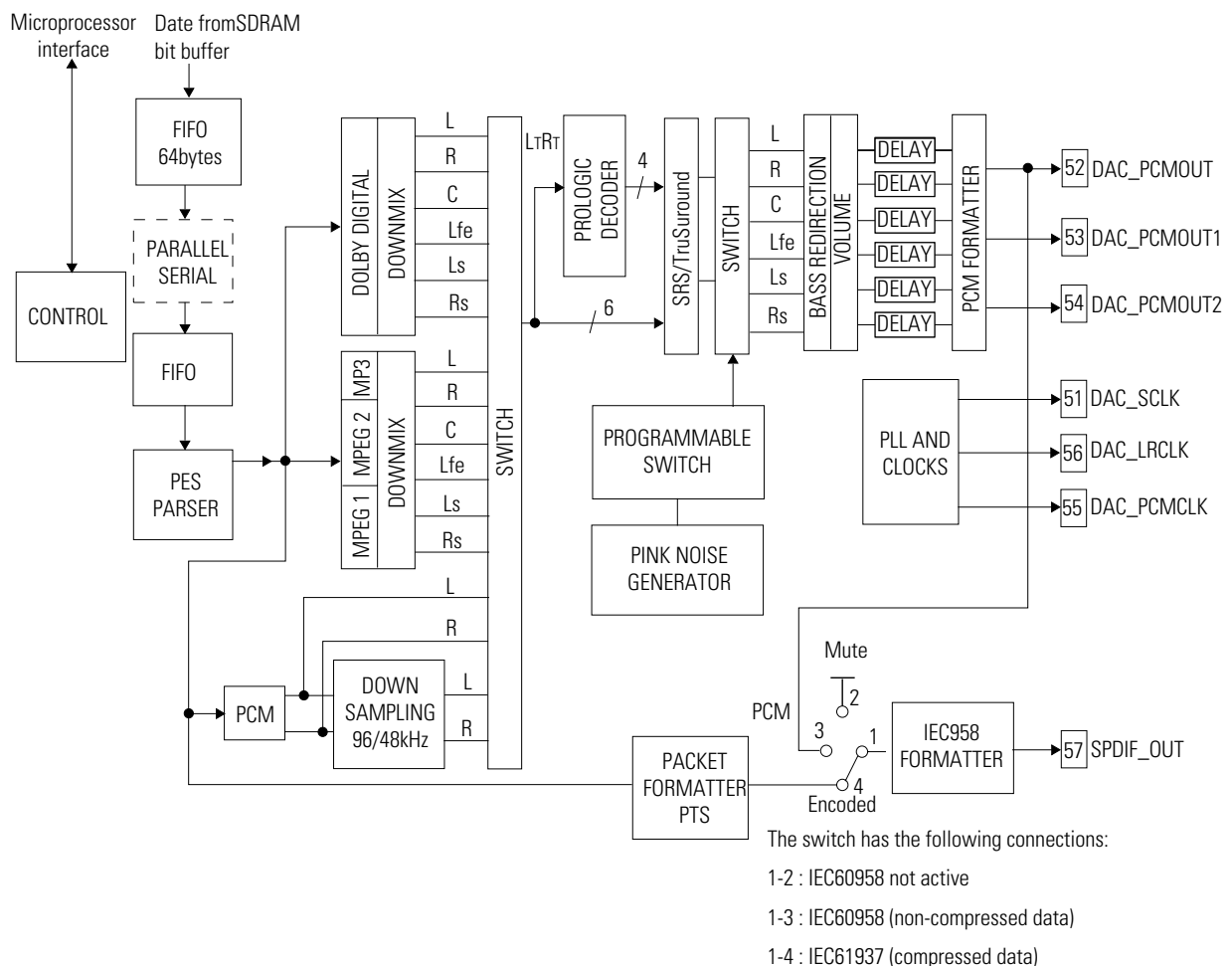


Fig 13-9 Audio decoder block diagram

2) Audio DAC

The audio digital to analog converter is a high performance stereo audio converter which accepts a 24-bit serial data stream from the MMDSP macro block and converts it into a current source analog output signal. This signal is then filtered and transformed into a 1.1 VRMS output signal by an external analog filter.

Fig 13-9 : Audio DAC outputs signals.

Table 13-2

Input/output	Pin name	Description
O	OUTPRIGHT	Right channel, differential positive analog output. The signal is then filtered.
	OUTMRIGHT	Right channel, differential negative analog output. The signal is then filtered.
	OUTPLEFT	Left channel, differential positive analog output. The signal is then filtered.
	OUTMLRIGHT	Left channel, differential negative analog output. The signal is then filtered.
I/O	LREF	DAC reference current. This pin should be connected to an external resistor.
	VBGFIL	DAC filtered reference voltage This pin should be connected to an external capacitor.

13-2-7 Digital encoder(DENC)

This the final stage of the video pipeline of the device is a high performance PAL/SECAM/NTSC digital encoder referred to as the DENC. The DENC converts a 4:2:2 digital video stream into a standard analog baseband PAL/SECAM/NTSC signal and into RGB and YUV analog components.

The DENC can perform closed captions, CGMS, WSS, teletext and VPS encoding and allows Macorvision™ 7.01/6.1 copy protection. Six analog output pins are available, on which it is possible to output one of the following:

- ◆ (S-VHS[Y/C] + CVBS + RGB)
- ◆ (S-VHS[Y/C] + CVBS + V + Y + U)
- ◆ (Y1 + C1 + CVBS1 + C2 + Y2 + CVBS2)

The encoder can operate in master mode or in one of several slave modes, where it locks on to incoming synchronous signals.

13-2-8 Memory Interface

1) Overview

The STi5517 has two memory interfaces.

The SMI is the STi5517's local memory interface and is used for all data requirements in unified memory applications, including graphics, video and audio buffers.

For high-performance, non-unified memory systems, additional data SDRAM can be placed on the EMI. Instructions can execute in place from flash on the EMI or can be copied to SDRAM on the SMI for unified memory applications or to SDRAM on the EMI for the highest performance systems.

2) Shared memory interface(SMI)

The SMI is a 16-bit wide data bus with a peak bandwidth of 270Mbyte/s. It supports one or two banks of 16-Mbit SDRAM, or one bank of 64-Mbit SDRAM, or one bank of 128-Mbit SDRAMs.

The SMI provides a fully cacheable address space for data and instructions, with data cacheability controlled 512Kbyte blocks for up to 8Mbytes. The STi5517 SMI bus is connected with U7(K4S641632H-TC75) 64-Mbit.

3) External memory interface(EMI)

This fourth generation EMI provides a glueless interface to SDRAM, SRAM, flash, SFlash™ and peripherals, in up to six configurable banks over a 16-bit wide interface. Bus cycles strobe timings can be programmed from 0 to 15 phases for slower peripherals. The EMI output drive of the STi5517 is programmable on a bus-by-bus basis, and connected with U8(K4S641632H-TC75) 64-Mbit.

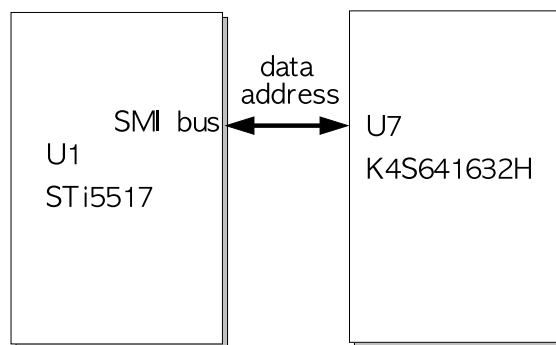


Fig 13-10 Memory interface block diagrams

13-2-9 Video Out

1) Overview

The STi5517 can be directed to six analog output pins through a 10-bit digital to analog converters operating at the reference clock frequency. The available output signals are :

S-VHS(Y/C)+CVBS+RGB, or S-VHS(Y/C)+CVBS+U+Y2+V, or Y1+C1+CVBS1+C2+Y2+CVBS2

Due to the 2.5V power supply used, the output swing of the DACs is about 1V p-p. Therefore some external gain may be required, which combined with the recommended output filtering stage, means active filtering.

For this active filtering stage to be very simple, it is possible to “invert” the DAC outputs by programming a bit of DEN, CFG5. Code N becomes code 1024-N, the result waveform undergoes a symmetry around the mid-swing code.

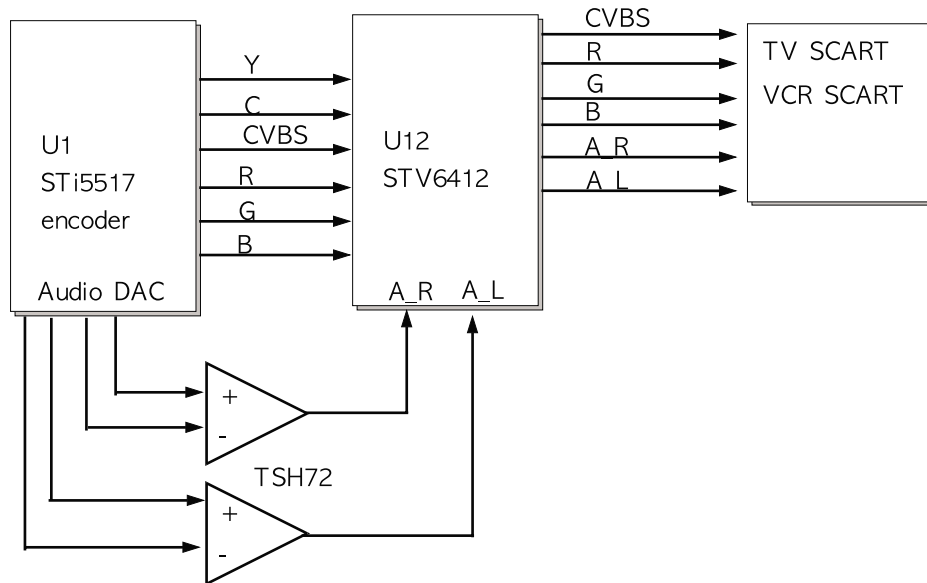


Fig 13-11 Video and Audio output block diagram

2) STV6412

The STV6412A is a highly integrated I2C bus-controlled audio and video switch matrix, optimized for use in digital application. It has 4 CVBS and 3 CVBS output, 6dB Gain on all CVBS Outputs.

13-2-10 Audio Out

The audio DAC provides differential current source outputs for each channel. The use of a differential mode interface circuit is recommended to achieve the best signal to noise ratio performance. So output is connected to symmetrical op-amp (TSH72) IC. and The audio signal output is connected with audio and video switching IC (STV6412).

13-2-11 Tuner

1) Overview

This tuner is a real part number TCMU30312PJT(C). This TCMU30312PJT(C) is adaptable to Digital CATV Set Top Box(STB) and NIM (Network Interface Module)Type.

It's consists of Tuner Block part with RF input frequency from 51 to 858MHz and IF AMP part of amplifier IF Frequency (36.125MHz),and QAM-Demod IC modulate a QAM-SIGNAL.

2) Tuner Block

This Block select a Channel from 51 to 858MHz Digital CATV signals.After frequency amplification and conversion,IF 36.125MHz (IF : Inter- mediate Frequency) out.

3) IF AMP Block

This AMP block is broadband amplifier that the 36.125MHz IF Signal is routed to QAMDEMOD IC.

4) QAM-DEMOM

QAM-demodulation IC send DATA[0:7], SYNC, ERROR,and VALID,CLOCK to MPEG DEMUX IC.

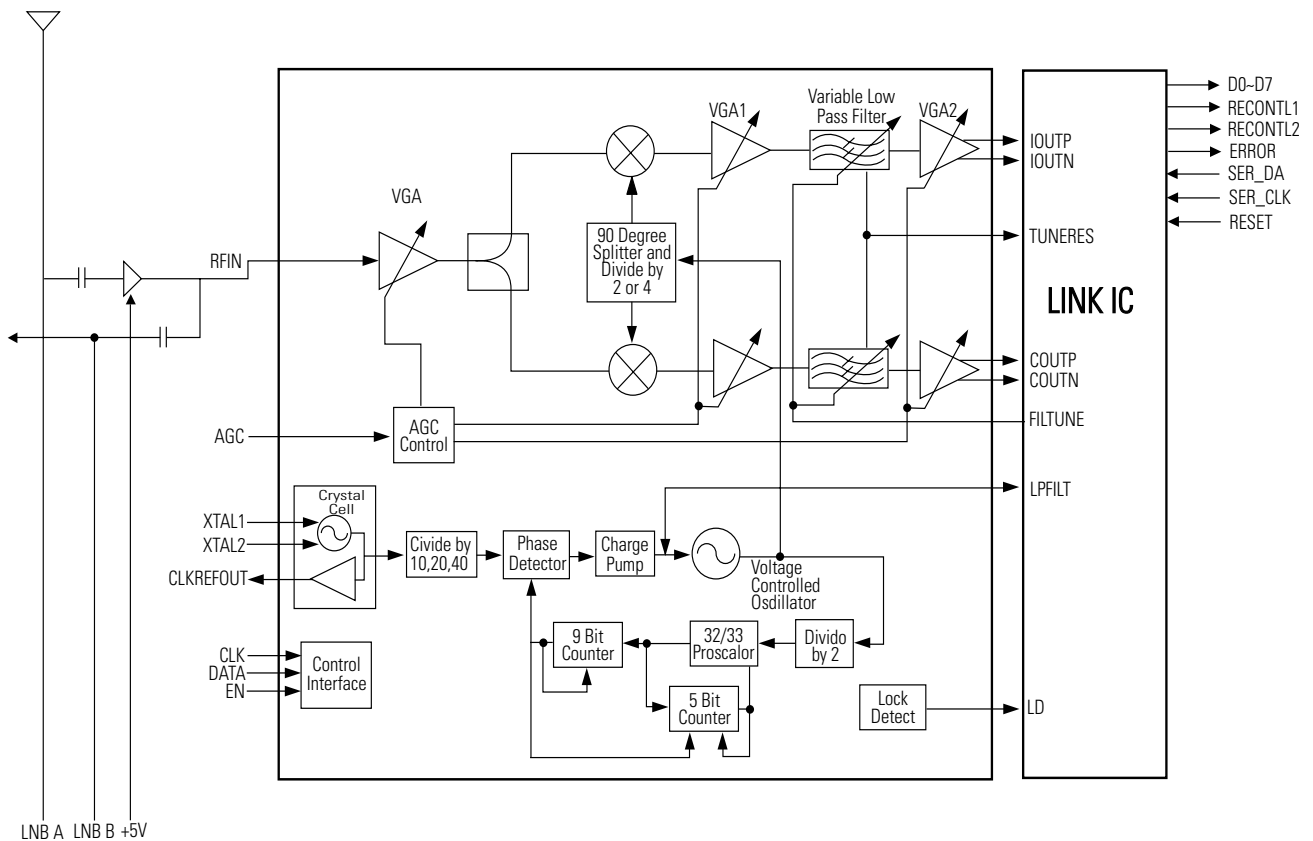


Fig 13-12 Tuner block diagram

13-2-12 Smart Cards

The TDA8024AT, IC card interface chip is compatible ISO 7816 Standards. It can be placed between the card and microcontroller to perform all supply, protection and control functions.

Power supply should be in the range of 2.7 to 6.5V. The internal DC/DC converter is incorporated to generate the 5V or 3V card supply voltage (Vcc).

The card clock signal (CLK) is derived from a clock signal input to pin XTAL1.

After power on and after internal pulse width delay, the system microcontroller can check the presence of a card using the signals /OFF and /CMDVCC. Fig 13-13 illustrates the sequence of activation.

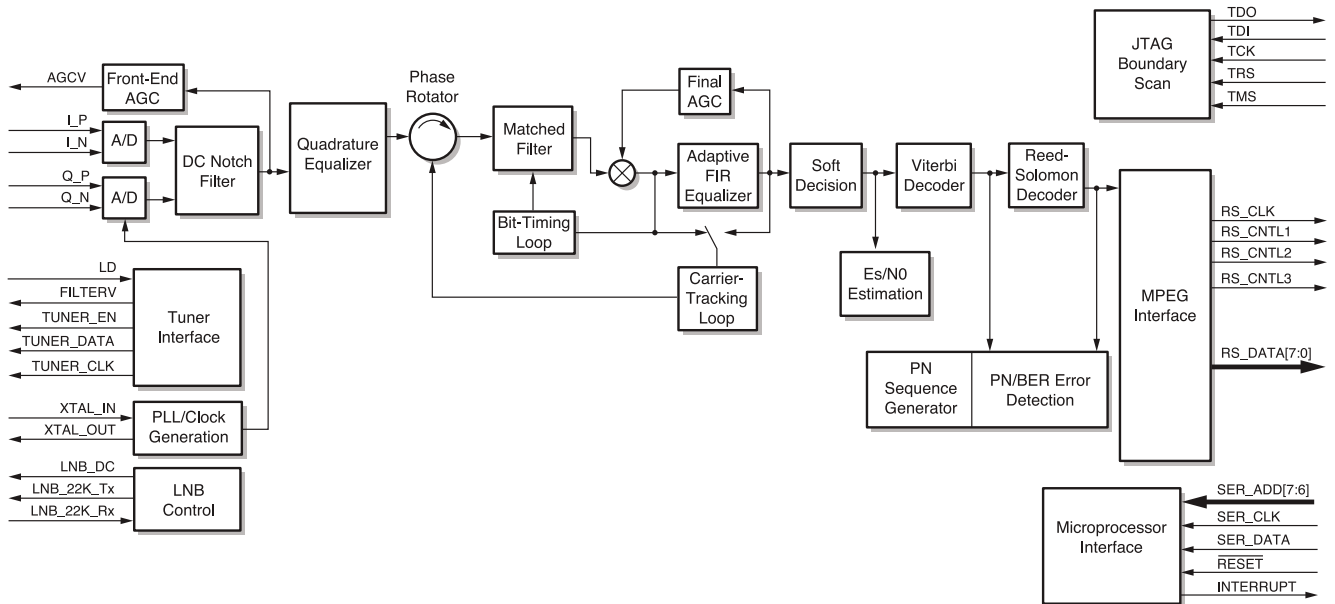


Fig 13-13 Illustrates the sequence of activation.